ABSTRACT OF THE DISCLOSURE

When a set signal goes high, a gate-source voltage is stored by an input capacitor such that an NMOS transistor maintains a source potential at a drain current. Next, when a set signal goes low and a write signal goes high, the NMOS transistor performs a source-follower operation and enters a stable state while charging a load capacitor. At timing when writing into the load capacitor is finished, the set signal and the write signal are put into low states. By doing this, the writing voltage is stored by the load capacitor. At the same time, current sources are forcibly turned off and the flow of a very small amount of bias current completely stops so that no power is consumed.